REMARKS

Claim 1 is revised to incorporate the substance of now-cancelled Claims 6 and 9. Claims 1-5, 7, 8, and 10 remain, with no claim previously allowed.

The objection to the drawings as failing to include certain reference numerals is noted. The corrected drawing sheets submitted herewith include those numerals and are believed to overcome that objection.

The objection to the specification and to the drawings for the use of labels HLS and HLZS is noted. The acronym "HLS" is an abbreviation for the German word "*Halbleiterschicht*", which in English is --semiconductor layer--. The acronym "HLZS" means "*Halbleiterzwischenschicht*", which in English is --semiconductor intermediate layer--. The present revisions to page 6 of the specification identify those meanings for the respective acronyms, and the specification as thus amended provides support for the use of those labels in the drawing figures.

Claims 1, 2, 4, 6, and 9 were rejected as anticipated by *Katoh* (US 5,041,882). The Applicant respectfully traverses that rejection as applied to Claim 1, now incorporating the substance of Claims 6 and 9, as well as Claims 2 and 4.

Claim 1, as currently amended, defines a heterobipolar transistor characterized by a gradual decrease of the band gap between the first (9) and the second (8) semiconductor layers (the reference-number identifications of those layers being shown in revised Fig. 3, submitted herewith). In contrast, *Katoh* discloses a gradual decrease of the band gap in an emitter layer 6 made of InGaAsP between the emitter layer 7 made of InP and the base layer 5 (see Fig. 1 and column 3, lines 22-27 of *Katoh*). The gradual decrease of the band gap according to the present

invention is provided on the contact side of the emitter, while *Katoh* discloses his band gap variation at the opposite sides of the emitter, namely, the base side.

The layers in the embodiment of Fig. 3 of the present application correlate as follows with the layers in Fig. 1 in *Katoh*:

- The first semiconductor layer (9) in Fig. 3 of the application corresponds to the emitter cap layer 9 in Fig. 1 of *Katoh*.
- The stacked semiconductor layers (31, 32, 33) in Fig. 3 of the application correspond to the emitter layer 8 in Fig. 1 of *Katoh*.
- The second semiconductor layer (8) in Fig. 3 of the application corresponds to the emitter layer 7 in Fig. 1 of *Katoh*.
- The further semiconductor layer (7) — introduced in Claim 10 — in Fig. 3 of the application corresponds to the emitter layer (6) in Fig. 1 of *Katoh*.
- The base layer (5) in Fig. 3 of the application corresponds to the base layer (5) in Fig. 1 of *Katoh*.

Summarizing the foregoing, in *Katoh* the gradual decrease of the band gap is provided in the emitter layer (6), while a gradual decrease of the band gap according to the present invention is established in the stacked semiconductor layers (31, 32, 33) as illustrated in the embodiment of Fig. 3. The advantage of the transistor according to Claim 1 is a lower resistance for the electrons to tunnel from the emitter contact layer to the emitter. *Katoh* fails to disclose the gradual decrease of the band gap in the stacked semiconductor layers as recited in Claim 1, and fails to provide the advantage arising from that structural arrangement. Accordingly, *Katoh* fails to anticipate a heterobipolar transistor characterized by the elements of Claim 1 and of the claims depending therefrom.

Dependent Claim 2 further characterizes the intermediate layer semiconductor material of the parent claim. Claim 3 depends from Claim 2 and specifies the band gap value of the intermediate layer semiconductor. Dependent Claims 4 and 5 characterize the particular materials comprising the first and second semiconductor materials and (in Claim 5) the intermediate layer semiconductor material. These claims further particularize the present invention with limitations missing from *Katoh*, and the claims define novel structure over that reference.

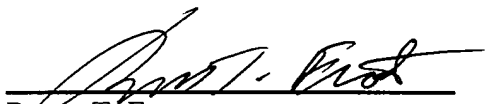
Claims 3, 5, and 7 were rejected as unpatentable over *Katoh*. Nothing in that reference discloses or suggests rearranging the layers in *Katoh* to provide the novel structural arrangement, or the resulting improved performance, discussed above and set forth in parent Claim 1. Accordingly, a semiconductor as defined in those dependent claims would not have been obvious to one of ordinary skill in the art.

Claims 8 and 10 were rejected as unpatentable over *Katoh* in view of *Schetzina* (US 5,679,965). The Applicant respectfully traverses that rejection. Nothing in the secondary reference teaches or suggests changing *Katoh* to comply with the limitations of parent Claim 1 and, indeed, the secondary reference was not cited for that purpose. Accordingly, dependent Claims 8 and 10 would not have been obvious to one of ordinary skill in the art at the time the Applicant made the present invention.

The foregoing is submitted as a complete response to the Office action identified above. The Applicant submits that the application is now in condition for allowance and solicits a notice to that effect.

Respectfully submitted,

MERCHANT & GOULD



Roger T. Frost
Reg. No. 22,176

Date: December 11, 2006

Merchant & Gould, LLC
P.O. Box 2903
Minneapolis, MN 55402-0903
Telephone: 404.954.5100

23552
PATENT TRADEMARK OFFICE